IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	David A. Luick	:	Date: July 19, 2006
Group Art Unit:	2113	:	IBM Corporation
Examiner:	C. McCarthy	:	Intellectual Property Law
Serial No.:	10/667,097	:	Dept. 917, Bldg. 006-1
Filed:	September 18, 2003	:	3605 Highway 52 North
Title: MULTIPLE PARALLEL PIPELINE PROCESSOR HAVING SELF-REPAIRING CAPABILITY		:	Rochester, MN 55901

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDMENT

This paper is being filed in response to the Office Action dated July 7, 2006. Please amend the above-identified application as follows.

Amendments to the Claims

Please cancel claims 8 and 16. Please amend claims 1 and 12. The currently pending claims are listed below.

1. (Currently Amended) A digital data processing apparatus, comprising:

at least one processor, each said at least one processor executing at least one respective thread of processor-executable instructions, said at least one processor collectively including:

(a) a plurality of parallel pipelines, each pipeline of said plurality of parallel pipelines having the capability to perform a set of pre-defined functions on respective input data; and

(b) control logic controlling the routing of data to said plurality of parallel pipelines, wherein said control logic, responsive to detection of a failure of a first pipeline of said plurality of parallel pipelines, causes data intended for processing by said first pipeline to be processed by a second pipeline of said plurality of parallel pipelines;

wherein said plurality of pipelines is arranged in an array;

wherein said control logic, responsive to detection of a failure in said first pipeline, causes data intended for processing by said first pipeline to be processed by said second pipeline, said second pipeline being physically adjacent said first pipeline in said array; and

wherein said control logic, responsive to detection of a failure in said first pipeline, further causes data intended for processing by said second pipeline to be processed by a third pipeline of said plurality of parallel pipelines, said third pipeline being physically adjacent said second pipeline in said array..

2. (Original) The digital data processing apparatus of claim 1, wherein said plurality of parallel pipelines comprises at least one redundant pipeline.

3. (Original) The digital data processing apparatus of claim 2, wherein said plurality of parallel pipelines comprises N primary pipelines and a single redundant pipeline, said redundant pipeline providing redundant function in the event of failure of any single one of said N primary pipelines, where N is greater than 1.

4. (Original) The digital data processing apparatus of claim 1, wherein said control logic comprises selection logic at one or more inputs to each respective pipeline, said selection logic controlling the selection between a primary source and a secondary source of pipeline data for the respective pipeline.

5. (Original) The digital data processing apparatus of claim 4, wherein said selection logic is integrated with operand source selection logic for one or more stages of the respective pipeline.

6. (Original) The digital data processing apparatus of claim 1, wherein said at least one processor is a plurality of processors, said plurality of processors sharing at least one of said plurality of parallel pipelines.

7. (Original) The digital data processing apparatus of claim 6, wherein said plurality of processors shares a redundant pipeline of said plurality of parallel pipelines.

8. (Cancelled)

9. (Original) The digital data processing apparatus of claim 1, wherein said plurality of parallel pipelines perform arithmetic operations on floating point data.

10. (Original) The digital data processing apparatus of claim 9, wherein said plurality of parallel pipelines perform arithmetic operations on mixed data, including floating point data and fixed point data.

11. (Original) The digital data processing apparatus of claim 1, further comprising:

a plurality of processors;

a memory storing instructions for execution on said plurality of processors; and

at least one bus coupling said plurality of processors to said memory.

12. (Currently Amended) A processor, comprising:

a plurality of parallel pipelines, each pipeline of said plurality of parallel pipelines having the capability to perform a set of pre-defined functions on respective input data, said plurality of parallel pipelines including at least one redundant pipeline; and

control logic controlling the routing of data to said plurality of parallel pipelines, wherein said control logic, responsive to detection of a failure of a first pipeline of said plurality of parallel pipelines, causes data intended for processing by said first pipeline to be processed by a second pipeline of said plurality of parallel pipelines;

wherein said plurality of pipelines is arranged in an array;

wherein said control logic, responsive to detection of a failure in said first pipeline, causes data intended for processing by said first pipeline to be processed by said second pipeline, said second pipeline being physically adjacent said first pipeline in said array; and

wherein said control logic, responsive to detection of a failure in said first pipeline, further causes data intended for processing by said second pipeline to be processed by a third pipeline of said plurality of parallel pipelines, said third pipeline being physically adjacent said second pipeline in said array.

13. (Original) The processor of claim 12, wherein said plurality of parallel pipelines comprises N primary pipelines and a single redundant pipeline, said redundant pipeline providing redundant function in the event of failure of any single one of said N primary pipelines, where N is greater than 1.

14. (Original) The processor of claim 12, wherein said control logic comprises selection logic at one or more inputs to each respective pipeline, said selection logic controlling the selection between a primary source and a secondary source of pipeline data for the respective pipeline.

15. (Original) The processor of claim 14, wherein said selection logic is integrated with operand source selection logic for one or more stages of the respective pipeline.

16. (Cancelled)

17. (Original) The processor of claim 12, wherein said plurality of parallel pipelines perform arithmetic operations on floating point data.

18. (Original) The processor of claim 17, wherein said plurality of parallel pipelines perform arithmetic operations on mixed data, including floating point data and fixed point data.

REMARKS

In an Office Action dated July 7, 2006, the Examiner rejected claims 1-3, 6-7, 9-13 and 17-18 under 35 U.S.C. §102(e) as anticipated by Akrout et al. (US 6,785,841), and rejected claims 4-5 and 14-15 under 35 U.S.C. §103(a) as unpatentable over *Akrout* in view of Dye (US 6,412,061). Claims 8 and 16 were objected to as dependent on respective rejected base claims, but otherwise indicated to contain allowable subject matter.

Applicants have amended independent claims 1 and 12 to incorporate all the limitations from dependent claims 8 and 16, respectively. As amended, independent claims 1 and 12 are of the same scope as original claims 8 and 16, respectively, although in independent form. Since claims 8 and 16 contain patentable subject matter, amended claims 1 and 12 are allowable. Dependent claims 8 and 16 have accordingly been cancelled as superfluous.

In view of the foregoing, applicants submit that the claims are now in condition for allowance and respectfully requests reconsideration and allowance of all claims. In addition, the Examiner is encouraged to contact applicants' attorney by telephone if there are outstanding issues left to be resolved to place this case in condition for allowance.

Respectfully submitted,

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